CLAIMS

We Claim:

1. A power amplifier circuit comprising:

a first amplifier configured to receive an input signal, and in response, provide a first output signal;

a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal;

a second amplifier configured to receive the delayed input signal, and in response, provide a first delayed output signal;

an impedance inverter circuit configured to provide impedance inversion and introduce a second delay to the first output signal, thereby creating a second delayed output signal;

means for combining the first and second delayed output signals, thereby creating an amplified output signal (RF_{OUT}); and

a bias control circuit configured to provide a first bias voltage ($BIAS_3$) that causes the first amplifier operate in a linear mode when the first amplifier is enabled, and a second bias voltage ($BIAS_4$) that causes the second amplifier to operate in a linear mode when the second amplifier is enabled.

2. The power amplifier of Claim 1, wherein the bias control circuit comprises:

means for activating the first bias voltage and deactivating the second bias voltage when a control signal identifies a low power mode; and

means for activating both the first and second

bias voltages when the control signal identifies a high power mode.

3. The power amplifier of Claim 1, wherein the means for combining comprise an output terminal configured to receive the first and second delayed output signals, wherein an output signal (RF_{OUT}) is provided on the output terminal.

4. The power amplifier of Claim 1, further comprising an impedance matching circuit, wherein the input signal is provided to the first amplifier and the delayed input signal is provided to the second amplifier through the impedance matching circuit.

5. The power amplifier of Claim 4, further comprising an input amplifier stage, wherein the input signal is provided to the first amplifier and the delayed input signal is provided to the second amplifier through the input amplifier stage.

6. The power amplifier of Claim 1, wherein the first delay circuit comprises an impedance inverter circuit.

7. The power amplifier of Claim 6, wherein the first amplifier exhibits a first impedance optimum load, and the second amplifier exhibits a second impedance optimum load, and the impedance inverter circuit exhibits a characteristic impedance equal to the first impedance.

8. The power amplifier of Claim 1, wherein the first delay is equal to the second delay.

9. The power amplifier of Claim 1, wherein the first amplifier comprises a first set of transistors, and the second amplifier comprises a second set of transistors.

10. The power amplifier of Claim 9, wherein the first set of transistors are coupled to receive the first bias voltage, and the second set of transistors are coupled to receive the second bias voltage.

11. The power amplifier of Claim 9, wherein a first subset of the first set of transistors are coupled to receive the first bias voltage, a second subset of the first set of transistors are coupled to receive the second bias voltage, and the second set of transistors are coupled to receive the second bias voltage.

12. The power amplifier of Claim 1, further comprising

a third amplifier configured to receive an input signal, and in response, provide a second output signal; and

a third delay circuit configured to introduce the second delay to the second output signal, thereby creating a third delayed output signal;

wherein the means for combining combines the first, second and third delayed output signals, thereby creating the amplified output signal, and the bias control circuit is configured to provide a third bias voltage ($BIAS_B$) that causes the third amplifier operate in a linear mode when the third amplifier is enabled.

13. A method of amplifying an input signal (RF_{IN}), comprising:

providing the input signal (RF_{IN}) to a first amplifier;

enabling the first amplifier to operate in a linear mode, such that the first amplifier provides a first output signal in response to the input signal;

introducing a first delay to the input signal, thereby creating a delayed input signal;

providing the delayed input signal to a second amplifier;

enabling the second amplifier to operate in a linear mode, wherein the second amplifier provides a first delayed output signal in response to the delayed input signal;

introducing a second delay to the first output signal, thereby creating a second delayed output signal; and

combining the first and second delayed output signals, thereby creating an amplified output signal (RF_{OUT}).

14. The method of Claim 13, further comprising selecting the first delay to be equal to the second delay, such that the first and second delayed output signals are substantially in phase.

15. The method of Claim 13, further comprising disabling the second amplifier in a low power mode.

16. The method of Claim 13, further comprising introducing the second delay with an impedance inverter circuit.

17. The method of Claim 16, further comprising selecting a characteristic impedance of the impedance inverter circuit to be equal to an optimum load impedance of the first amplifier.

18. The method of Claim 13, further comprising:

providing the input signal to the first amplifier through an impedance matching circuit; and

providing the delayed input signal to the second amplifier through the impedance matching circuit.

19. The method of Claim 18, further comprising:

providing the input signal to the first amplifier through an input amplifier stage; and

providing the delayed input signal to the second amplifier through the input amplifier stage.

20. The method of Claim 13, wherein the steps of enabling the first and second amplifiers further comprise:

applying a first bias voltage to a first set of transistors in the first amplifier; and

applying a second bias voltage to a second set of transistors in the second amplifier.

21. The method of Claim 20, wherein the step of enabling the first amplifier further comprises applying the second bias voltage to a third set of transistors in the first amplifier.

22. The method of Claim 13, further comprising:

providing the input signal (RF_{IN}) to a third amplifier;

enabling the third amplifier to operate in a linear mode, such that the third amplifier provides a third output signal in response to the input signal;

introducing a third delay to the third output signal, thereby creating a third delayed output signal; and

combining the first, second and third delayed output signals, thereby creating an amplified output signal (RF_{OUT}).